

Design and Analysis of CMOS Telescopic OTA for 180nm Technology

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Abstract

In this paper, different types of OTA topologies are compared for their suitability to be used in Sigma-Delta modulator. The most suitable OTA for Sigma-Delta modulator, telescopic OTA is designed and implemented. The designed telescopic OTA has gain of 52.788db, phase margin of 59.44 deg, power consumption of 61.49μW at a power supply of 3V.

Keywords: Telescopic OTA, Single stage OTA, two stage OTA, folded cascode OTA.

I. Introduction

The Band-pass Sigma-Delta ADC are usually implemented by switched-capacitor (SC) [1] technique. However, SC implementations are limited in that the sampling frequency of the modulators cannot be too high (below 50MHz).

Even using the double-sampling technique[2] or 2-path technique [3], the center frequency of the band-pass signal is still limited to below 50 MHz. As mentioned above discrete-time system or switched-capacitor band-pass Sigma-Delta modulator cannot operate above 50MHz. To achieve frequencies above 50MHz a continuous-time filter is needed.

In this paper we presents the design and measurement of a telescopic OTA. The described telescopic OTA [4] is used for the design of sigma-delta modulator in transceiver[5]. The OTA should have the properties as low power, high gain, high speed and low noise for the sigma-delta modulator[5]. As the design targets in[4], the gain to be 59.44db, power consumption 61.49μW, at a frequency of 70MHz for power supply of 3V. The different types of OTA and different architectures[4] is described in section II. The experimental results of the telescopic OTA are presented in Section III. Finally, we summarize and conclude our work.

II. Operational Transconductance Amplifier

A. Introduction

The input and output of an OTA are voltage and current, respectively. The OTA is often used in open loop. Its

transconductance gain is G_m . The OTA input and output impedances are ideally infinite. Integrators implemented with an Op Amp, R and C have a time Constant equals to RC. There is ideally no effect of the Op Amp. Integrators with an OTA and a C have time constant equals to G_m/C .

OTA's in general operate at higher frequencies than Op Amps because they have low impedance internal nodes, and operate in open loop.

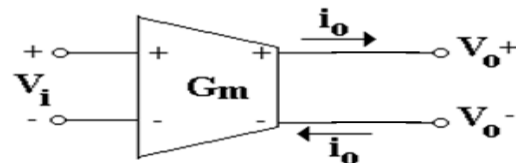


Fig 1: OTA symbol [4]

An operational transconductance amplifier (OTA) is a voltage input, current output amplifier.

The input voltage V_{in} and the output current I_o are related to each other by a constant of proportionality and the constant of proportionality is the transconductance "gm" of the amplifier.

$$I_o = g_m * V_{in} \quad (1)$$

Where g_m = transconductance of OTA
 V_{in} = differential input voltage

The transconductance g_m of the OTA can be varied by varying the value of the external controlling current I_c .

$$G_m = K I_c \quad (2)$$

Where K = suitable constant of proportionality

The I_o is given as:

$$I_o = K V_{in} I_c \quad (3)$$

Above equation tells us that output current is proportional to the product of V_{in} and I_c . Actually OTA consist of a

differential transistor pair with a current mirror circuit acting as a load. Since OTA operates on the principle of processing current rather than voltage, it is an inherently fast device. As gm can be controlled by changing the control current Ic, the OTA are suitable to electronically programmable functions.

B. Different OTA Topologies

1. Single Stage

Single stage OTA is as shown in fig 2. This single stage OTA is less complex compare to other types of OTA topology. Because of its less complex property its speed is higher compare to other topology. The drawback of this type of OTA is lower gain due to the fact that output impedance of this type configuration is relatively low. However this low impedance also leads to high unity gain bandwidth and high speed.

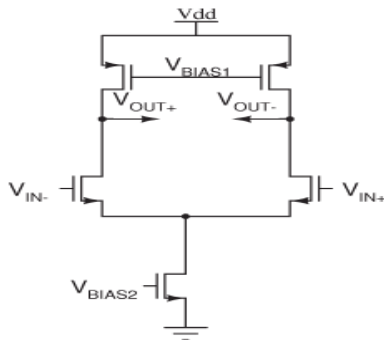


Fig 2: single stage [4]

2. Two stage OTA

As shown in fig.3 that is basic circuit diagram of two stage OTA. In which M1 and M2 use for differential input pair, M3 and M4 forms current mirror. The drawback of having limited gain of the single stage OTA is overcome by two stages OTA. In this type of configuration two stages are used. One of them provides high gain followed by second stage which provides high voltage swing. This modification increases the gain up to some certain extent compared to single stage OTA. But this addition of extra stage also increases complexity. And the increased complexity will reduce the speed in comparison to a single stage amplifier.

Advantages:

1. It has high output voltage swing.
2. It has higher gain compare to single stage OTA.

Disadvantages:

1. It has a compromised frequency response.
2. This topology has high power consumption because of two stages in its design.
3. It has a poor negative Power Supply Rejection at higher frequencies.

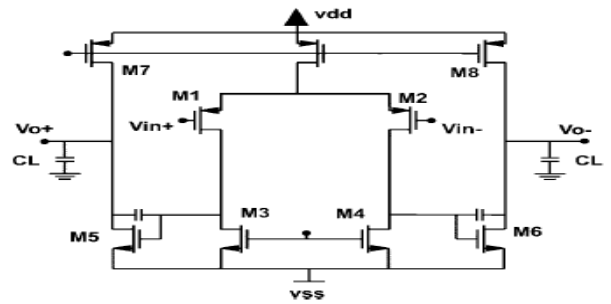


Fig 3: two stage OTA[4]

3. Telescopic OTA

The Telescopic OTA configuration is as shown in fig 4. Single Stage OTA have low gain due to fact that it has low output impedance, One way of increasing the impedance is to add some transistors at the output including using an active load. Transistors are stacked on top of each other. The transistors are called "cascode", and will increase the output impedance and thereby increase the gain.

Advantage:

- 1) It provides higher speed.
- 2) It has lower power consumption.

Disadvantage:

- 1) Limited output swing.
- 2) Shorting the input and output is difficult.

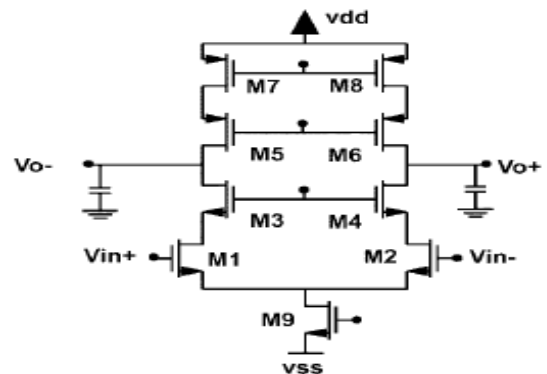


Fig 4: telescopic OTA[11]

4. Folded cascode OTA.

The folded cascode amplifier is in a way some sort of a compromise between the two-stage amplifier and the telescopic cascode amplifier. It permits low supply voltage, still having a rather high output voltage swing and the input and output common mode levels can be designed to be equal. Its gain is lower than for the two-stage and its speed is lower than for the telescopic cascode, which makes it a good compromise between these two amplifiers.

Advantage:

- 1) This design has corresponding superior frequency response than two-stage operational Amplifiers.
- 2) It has better high frequency Power Supply Rejection Ratio (PSRR). The power consumption of this design is approximately the same as that of the two-stage design.

Disadvantages:

- 1) Folded cascode has two extra current legs, and thus for a given settling requirement, they will double the power dissipation.
- 2) The folded cascode stage also has more devices, which contribute significant input Referred thermal noise to the signal.

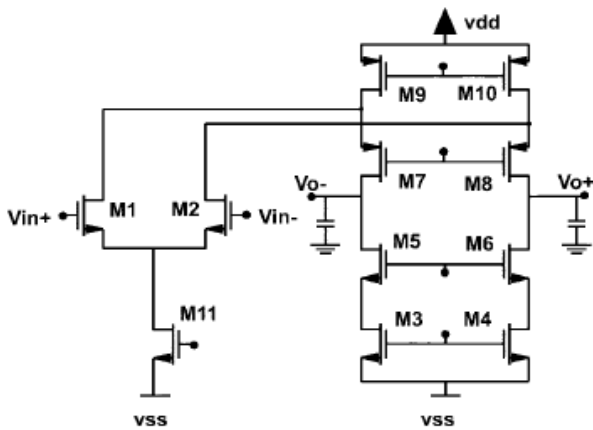


Fig 5: folded cascode OTA[4]

5. Comparison of different types of OTA

Table 1 shows the comparison of different types of OTA

| topology | Gain | power | speed | Noise |
|----------------|--------|--------|-------|-------|
| Single stage | Low | medium | high | High |
| Two stage | high | medium | low | high |
| Telescopic OTA | high | low | high | low |
| Folded cascode | medium | medium | high | high |

Table 1: comparison of different types of OTA

III. Design of Telescopic OTA

A telescopic OTA as shown in Fig.6, typically has higher frequency capability and consumes less power than other topologies. Its high-frequency response stems from the fact that its second pole corresponding to the source nodes of the n-channel cascode devices is determined by the transconductance of n-channel devices as opposed to p-channel devices, as in the case of a folded cascode. Also, the

parasitic capacitance at this node arises from only two transistors instead of three, as in the latter. The single stage architecture naturally suggests low power consumption. The disadvantage of a telescopic op-amp is severely limited output swing. It is smaller than that of the folded cascode because the tail transistor directly cuts into the output swing from both sides of the output.

In the telescopic op-amp shown in Fig.6, all transistors are biased in the saturation region. Transistors M1–M2, M7–M8, and the tail current source M9 must have at least to offer good common-mode rejection, frequency response, and gain. Table 2 shows the W/L ratios from calculation and table 3 shows the optimized W/L ratios for telescopic OTA.

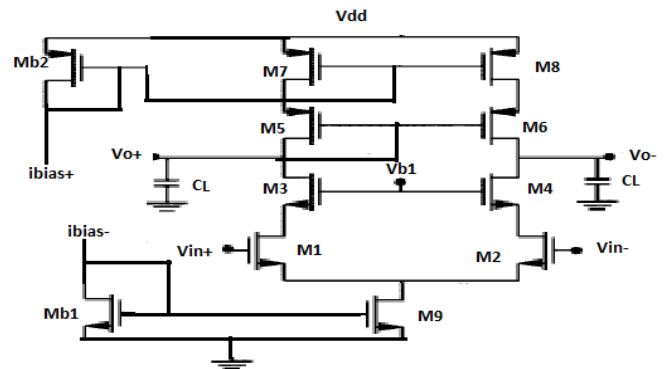


Fig 6: Schematic of the CMOS Telescopic OTA

Table 2: W/L ratio from calculation with respect 180nm length

| Transistor | Value of W/L ratio |
|-------------|--------------------|
| M1,M2,M3,M4 | 2μ/180nm |
| M5,M6,M7,M8 | 28.8μm/180nm |
| Mb2 | 360nm/180nm |
| Mb1,M9 | 190nm/180nm |

Table 3: Optimised W/L ratios of the telescopic OTA

| Transistor | Value of W/L ratio |
|-----------------|--------------------|
| M1,M2,Mb1,M9 | 15μm/180nm |
| M3,M4 | 20μm/180nm |
| M5.M6,M7,M8,Mb2 | 40μm/180nm |

1. Theoretical Calculation of Telescopic OTA

Let assume the slew rate of Telescopic OTA 10V/μs. The Load capacitance at the output is assumed to be 1pF. The slew rate is, $SR = I_b / C_1$

$$I_b = SR \cdot C_1 = 10 \cdot 1 \cdot 10^{-6}$$

- =10 μ A
- Design of M7,M8,M5 and M6,

$$\left(\frac{W}{L}\right)_7 = \frac{2I_b}{K'_7((V_{dd} - V_{in(max)}) - |V_{tp}|(max) + V_{tn}(min))^2}$$

Where K' is Transconductance parameter for nMOS,
 $k' = 110 \pm 10\% \mu\text{A}/\text{V}^2$ [11]
 For pMOS, $k' = 50 \pm 10\% \mu\text{A}/\text{V}^2$ [11].

$$\left(\frac{W}{L}\right)_7 = \frac{20 * 10^{-6}}{50 * 10^{-6}(((3 - 2.8) - 0.9 + 0.75))^2}$$

$$= \frac{20 * 10^{-6}}{50 * 10^{-9} * 2.5}$$

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = 160$$

- Design of M1,M2,M3 and M4

$$\left(\frac{W}{L}\right)_1 = \frac{gm_1^2}{K'_1 \cdot I_b}$$

Where gm_1 is transconductance of Transistor 1
 $gm_1 = GB \cdot C_l$

Where GB is gain bandwidth

$$gm_1 = 10.023 * 2\pi * 1 * 10^{-12} * 10^6$$

$$gm_1 = 62.94 \mu\text{s}$$

$$\text{Hence, } \left(\frac{W}{L}\right)_1 = \frac{62.94^2}{110 * 10}$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 3.60 \approx 4$$

- Design of Mb1 and M9

$$\left(\frac{W}{L}\right)_{Mb1} = \frac{2 * I_b^2}{K'_1 \cdot (V_{DSMb}(sat))^2}$$

IV. Experimental Results

The below figures shows the results of telescopic OTA:
 The figure 7 shows the test circuit of telescopic OTA,
 figure 8 shows the transient response of telescopic OTA
 at a time interval of 100ns, figure 9 shows the gain of
 telescopic OTA at a frequency of 70MHz, figure 10
 shows power analysis of telescopic OTA and figure 11
 shows phase margin of telescopic OTA.

The saturation voltage of transistor Mb is,

$$V_{DSM9}(sat) = V_{SS} - V_{in}(min) - \sqrt{\frac{I_b}{K'_1 \cdot \left(\frac{W}{L}\right)_1}} - |V_{tn}(max)|$$

$$V_{DSM9}(sat) = 0 - (-1.2) - \sqrt{\frac{10}{110 * 3.60}} - 0.9$$

$$= 0.142$$

$$\left(\frac{W}{L}\right)_{Mb1} = \left(\frac{W}{L}\right)_9 = \frac{20}{110 \cdot (0.142)^2} = 2.21$$

- Design of Mb2

$$\left(\frac{W}{L}\right)_{Mb2} = \frac{K'_n}{K'_p} \left(\frac{W}{L}\right)_{Mb1}$$

$$\left(\frac{W}{L}\right)_{Mb2} = 1.88 * 2.21 = 4.15$$

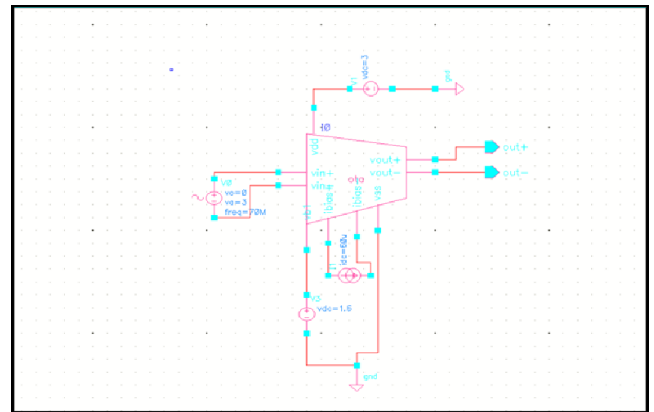


Fig 7: Test Circuit of Telescopic OTA

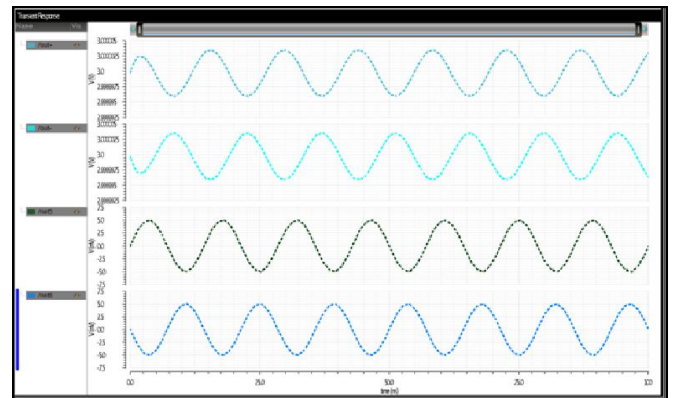


Fig 8: Transient response of telescopic OTA

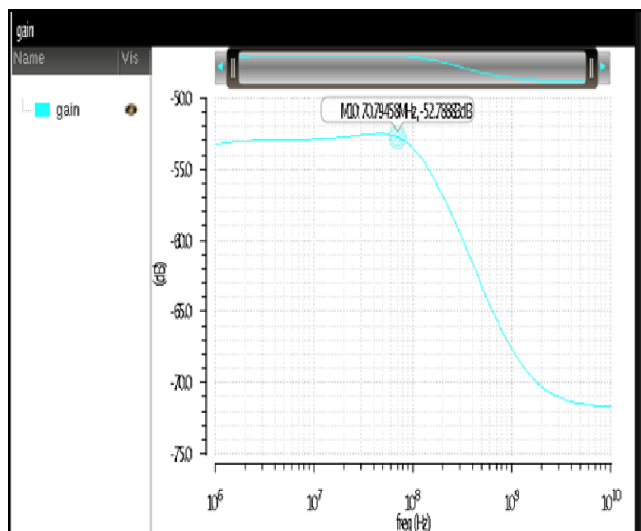


Fig 9: Gain of telescopic OTA

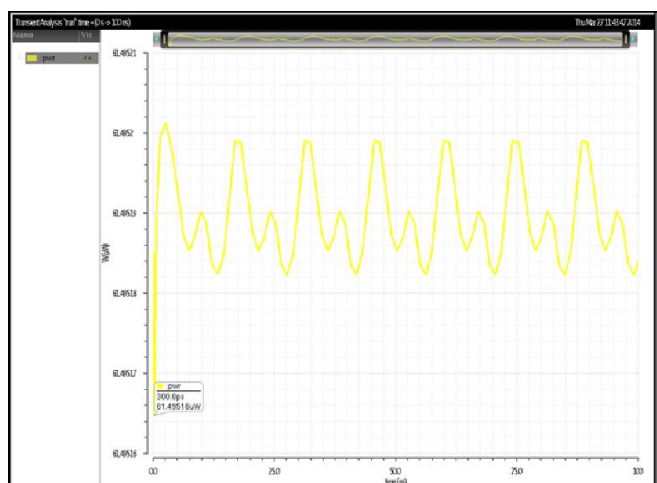


Fig 10: power analysis of telescopic OTA

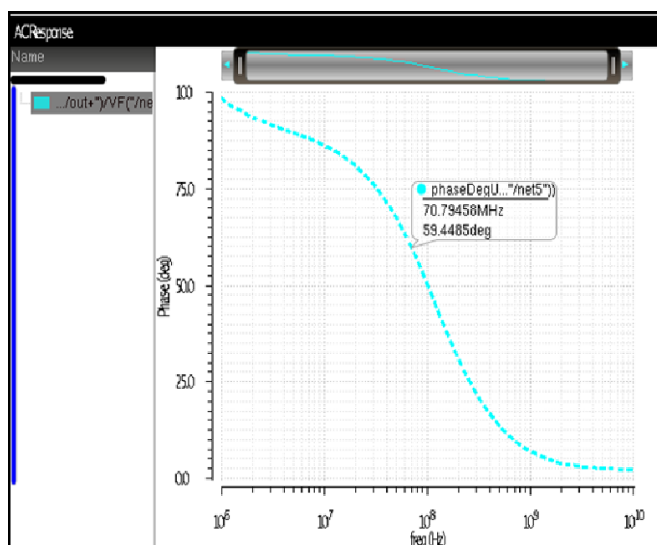


Fig 11: phase margin of telescopic OTA

Table 4 shows the summarized result of telescopic OTA

| Parameter | Telescopic OTA |
|-------------------|----------------|
| Phase Margin | 59.55deg |
| Power consumption | 61.49 μ W |
| Power | 3V |
| Gain | 52.788db |
| Technology | CMOS 180nm |
| Input frequency | 70MHz |

IV. Conclusion

The design and experimental results of a telescopic OTA has been presented. The proposed telescopic OTA can achieve a maximum gain of 52.788db, power consumption of 61.49 μ W at a power supply of 3V.

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References

- [1] W. Singor & W. M. Snelgrove, "Switched-Capacitor Bandpass Delta-Sigma A/D Modulation at 10.7 MHz", *IEEE J. of Solid-State Circuits*, vol. 30, no. 3, pp.184-192, March 1995.
- [2] S. Bazarjani & M. Snelgrove, "A 40 MHz IF Fourth-order Double-Sampled SC Bandpass Sigma-Delta Modulator", *Proceedings of IEEE International Symp. on Circuits & Systems*, June 1997.
- [3] A. K. Ong & B. A. Wooley, "A two-path bandpass Sigma Delta modulator for digital IF extraction at 20 MHz", *IEEE J. of Solid-State Circuits*, vol. 32, no. 12, pp.1920-34, Dec. 1997.
- [4] Kalpesh B. Pandya, Kehul A. shah "Design and analysis of CMOS telescopic operational transconductance amplifier for 0.35 μ m technology" international journal of science and research, volume 2, issue 3, page(s):87-90, march 2013.
- [5] Issac Hsu and Howard C. Luong. "A 70-MHz Continuous-time CMOS Band-pass $\Sigma\Delta$ Modulator for GSM Receivers" *ISCAS 2000 -IEEE International Symposium on Circuits and Systems*, Geneva, Switzerland, volume 3, page(s): 750-753, May 28-31, 2000.

- [6] Y. S. Shu, J. Kamiishi, K. Tomioka, K. Hamashita, and B. S. Song, "LMS based noise leakage calibration of cascaded continuous-time $\Sigma\Delta$ modulators," IEEE J. Solid-State Circuits, vol. 45, no. 2, pp. 368-379, Feb. 2010.
- [7] C. Y. Lu, J. F. Silva-Rivas, P. Kode, J. Silva-Martinez, and S. Hoyos, "sixth-order 200 MHz IF bandpass sigma-delta modulator with over 68dB SNDR in 10 MHz bandwidth, "IEEE J. Solid-State Circuits, vol. 45, no.6,pp. 1122-1136, June 2010.
- [8] Hamid Reza Sabouhi, Mohammad Honarparvar and Vahid Sabouhi, A 60- μ W, 98-dB SNDR and 100-dB Dynamic Range Continuous Time Delta Sigma Modulator for Biological Signal Processing in 0.18- μ m CMOS, Journal of Basic and Applied Scientific Research, 2012.
- [9] Nagaraj P, Siva yellampalli "8-bit second-order continuous-time band pass sigma-delta ADC" international journal of innovative technology and exploring engineering, volume 3, issue-1, page(s):106-111, june 2013.
- [10] Kush gulati and Hae-seung lee "A high-swing CMOS telescopic operational amplifier" IEEE journal of solid-state circuits, volume 33, no.12, page(s):2010-2019, December 1998.
- [11] Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 2nd edition, New York: Oxford University Press, 2004.